VS8812

HIGH DEFINITION VIDEO

TO

TV ENCODER

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1 OVERVIEW

1.1 DESCRIPTION

VS8812 is an advanced high definition video to TV encoder coversion chip. It consists of video input format converter, picture enhancement and color processing, and the any ratio vertical and horizontal scaler, video output format converter and standard TV encoder.

It receives any format of input, such as RGB 24 -bit, YUV 24-bit, YUV 16-bit and YUV 8-bit or CMOS Bayer format raw data. It can also process sync embedded input such as bt-656 or bt-1120 format. The input resolution can be interlace such as 480i, 576i, 1080i or progressive such as 480P, 576P, 720P, 1080P, 4K2K.

There are three analog DAC output pin, it can be configured as CVBS+S-video output, or three CVBS output simultaneously or YPbPr output or RGB output. The output format is standard TV NTSC or PAL analog format. With the embedded frame buffer, the VS8812 can perform any input frame rate conversion to 50/60 Hz frame output for NTSC/PAL format.

The VS8812 can perform high quality picture enhancement such as video noise reduction, sharpening, black-level / white-level extension, gamma correction, and brightness, contrast, saturation, hue processing. There are also font-based on-screen-display (OSD), with 64 programmable font to make it suitable for different video application.

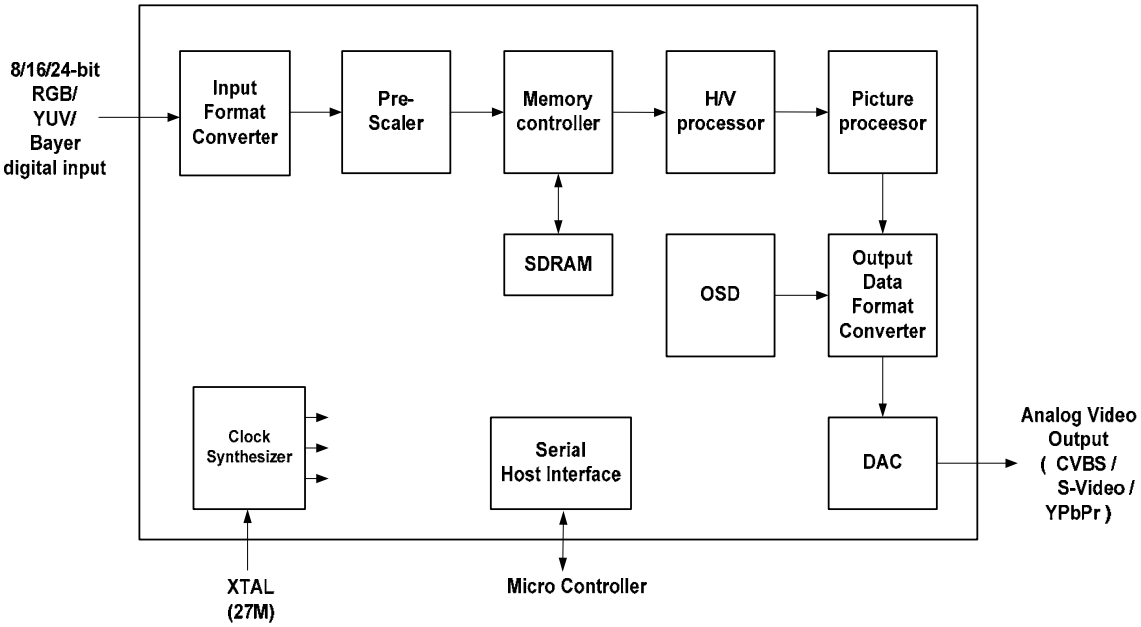
1.2 APPLICATION

- Video format converter to TV
  (ex. HDMI/VGA to TV converter)
- Surveillance (Sensor to TV converter)
- Car/Multimedia panel
- Set-top box

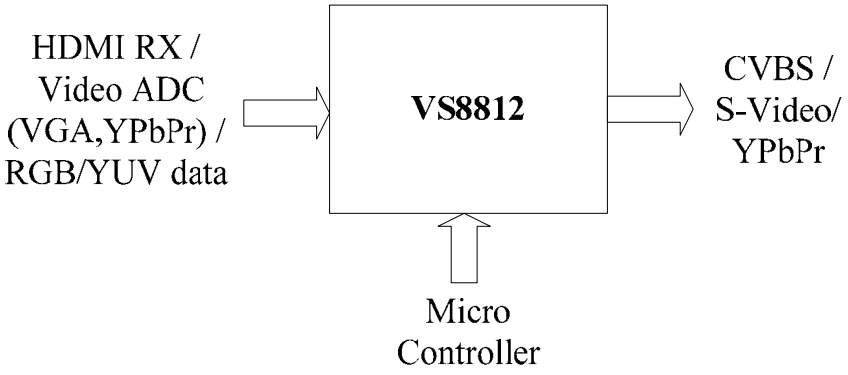
2 FEATURES

- Support Various Digital Video Input Formats
  - 8-bit interlace ITU-R BT.656
  - 8-bit progressive BT.656
  - 8-Bit ITU-R BT.601 + Horizontal Sync + Vertical Sync
  - 16-bit Y/UV input
  - 24-bit RGB/YUV progressive input
  - 8-bit CMOS Raw Bayer format input
  - BT.1120 16 bit input
- Resolutions of all input format are up to 1080P / 4K2K
- Support three NTSC/PAL Analog output
  - 1 CVBS + 1 S(Y,C) Video output
  - 3 CVBS output
  - YPbPr SD output
  - RGB SD output
- Frame rate up/down conversion
- 3D noise reduction
- Video Flip, Mirror, Still
- Auto white balance
- Embedded Scaling Engine (Relács), Supporting output Resolution from 320X240 to 1920X1080
- Brightness, Contrast, Saturation, and Hue Adjustment
- Color Transient Improvement, Adaptive Black-Level Extension, Skin Tone Enhancement.
- Frequency Directive Picture Sharpening
- 3-Channel 10-Bit Build-In Color gamma Look-Up Table for Video Fine-Tune
- Host Interface Compatible with Two-Wire IIC, Serial Interface
- OSD with 128 Build-in and 64 Programmable Font and Attribute Table, 16 Colors at same Time from 16,777,216-Color Template, Blinking, and Blending
- R/G/B input port swap & rotation control
- One 27MHz crystal needed
- 1.8V / 3.3V power supply with 3.3V digital I/O

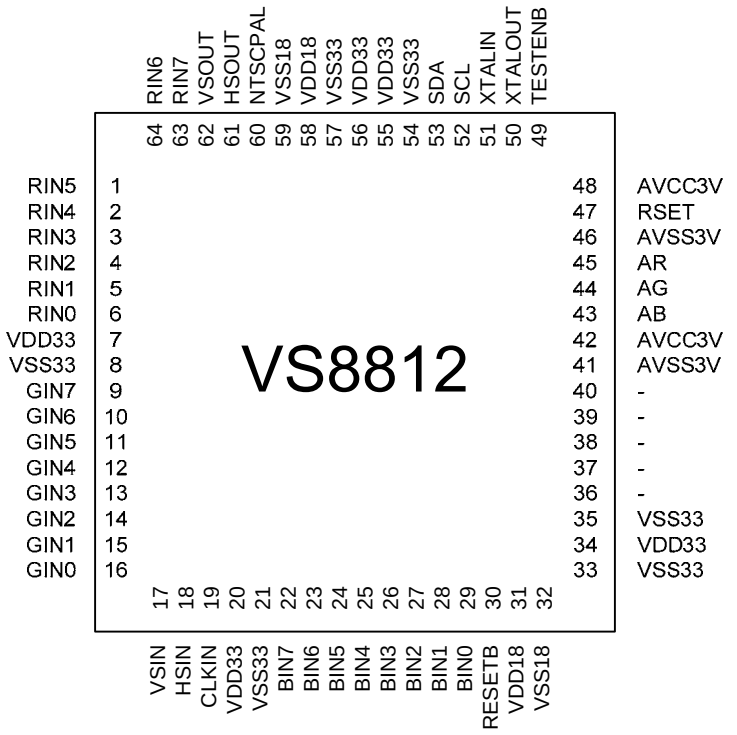
3 BLOCK DIAGRAM



4 APPLICATION



5 PINOUT DIAGRAM



6 PIN ASSIGNMENT

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name_	Pin #	Pin Name
1	RIN5	17	VSIN	33	VSS33	49	TESTENB
2	RIN4	18	HSIN	34	VDD33	50	XTALOUT
3	RIN3	19	CLKIN	35	VSS33	51	XTALIN
4	RIN2	20	VDD33	36	-	52	SCL
5	RIN1	21	VSS33	37	-	53	SDA
6	RIN0	22	BIN7	38	-	54	VSS33
7	VDD33	23	BN6	39	-	55	VDD33
8	VSS33	24	BIN5	40	-	56	VDD33
9	GIN7	25	BIN4	41	AVSS3V	57	VSS33
10	GIN6	26	BIN3	42	AVCC3V	58	VDD18
11	GIN5	27	BIN2	43	AB	59	VSS18
12	GIN4	28	BIN1	44	AG	60	NTSCPAL
13	GIN3	29	BIN0	45	AR	61	HSOUT
14	GIN2	30	RESETB	46	AVSS3V	62	VSOUT
15	GIN1	31	VDD18	47	RSET	63	RIN7
16	GIN0	32	VSS18	48	AVCC3V	64	RIN6

7 PIN DESCRIPTION

Video Input Pins

Name	Type	Description	Notes
RIN7~0	I	Red input data	
GIN7~0	I	Green/BT656/Bayer input data	
BIN7~0	I	Blue input data	
VSIN	I	Input Vertical Synchronization	
HSIN	I	Input Horizontal Synchronization	
CLKIN	I	Input Data Clock	

Video Output Pins

Name	Type	Description	Notes
HSOUT	O	Video Output Horizontal Synchronization / GPO1	
VSOUT	O	Video Output Vertical Synchronization / GPO0	

Analog Video Output Pins

Name	Type	Description	Notes
AR	O	S-Video Y / CVBS / R analog output	
AG	O	CVBS / G analog output	
AB	O	S-Video C / CVBS / B analog output	
RSET	A	DAC gain control pin	

Miscellaneous I/O Pins

Name	Type	Description	Notes
RESETB	I_{PU}	Chip Reset (Active Low)	
XTAL_OUT	XO	Crystal Output	
XTAL_IN	XI	Crystal Input	
SDA	I_{PU}/O	Host Interface Serial Data / Address	
SCL	I_{PU}	Host Interface Serial Clock	
TEST_ENB	I_{PU}	Test Mode Enable (Active Low)	
NTSCPAL	I_{PD}/ O	CVBS NTSC/PAL output Select / Clock output	

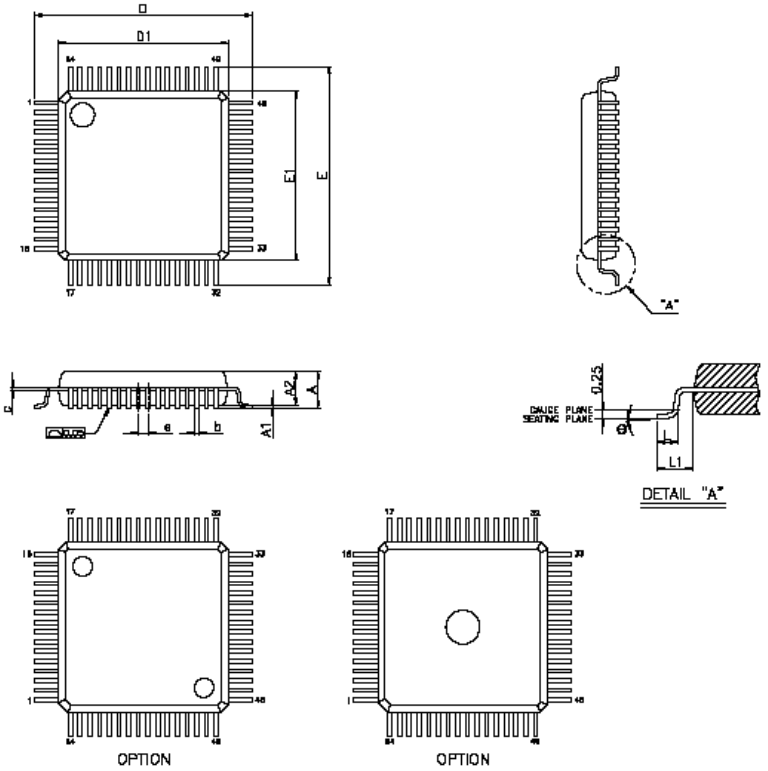
Power Pins

Name	Type	Description	Notes
VDD33	P_{33}	Digital 3.3V power for I/O	Qty: 5
VSS33	G	Digital Ground For I/O	Qty: 6
VDD18	P_{18}	Digital 1.8V Power for Core	Qty: 2
VSS18	G	Digital Ground for Core	Qty: 2
AVCC3V	P_{33}	Analog 3.3V power for DAC	Qty: 2
AVSS3V	G	Analog ground for DAC	Qty: 2

note :	
I	3.3V input
O	3.3V output
I/O	3.3V input/output
I_{PU}	3.3V input with internal pull up
XI,XO	crystal input, output pin
P_{33}	3.3V power pin
P_{18}	1.8V power pin
G	Ground pin

8 PACKAGE

■ VS8812 64-Pin LQFP



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D		9.00 BSC	
D1		7.00 BSC	
e		0.40 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:
1. JEDEC OUTLINE : MS-026 BBD
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.